WHAT IS CLAIMED IS:

1.   A processor having a register renaming function, comprising:

an instruction fetch part configured to fetch an instruction;

a decoding part configured to decode an instruction code from the instruction fetched by the instruction fetch part;

a register part configured to hold data corresponding to a register number indicated by the instruction code decoded by the decoding part;

a register body configured to hold data corresponding to a register number indicated by said instruction code;

a caching register configured to cache the contents held by said register body;

an inner instruction information holding part configured to hold information on a state of an inner instruction including a logical register number and a caching register number, which are held by said caching register by an instruction from said instruction fetch part;

an instruction insertion determining part configured to compare an instruction code, which is obtained by pre-decoding the instruction from said instruction fetch part, with information on a state of the inner instruction, which is held by said inner instruction information holding part, to determine whether the inner instruction is to be inserted; and

a register transfer instruction issuing part configured to issue a register transfer instruction for transferring inner data between said caching register and said register body when said instruction insertion determining part determines that the inner transfer instruction is to be inserted,

thereby the processor having a register renaming function for sequentially rewriting the contents of a

register alias table using a reorder buffer and a physical register free list, said reorder buffer holding a correspondence of a logical register number to its physical register number, which are included in the decoded instruction code, in a register alias table and storing an assignable number of the physical register number in the physical register free list to store a correspondence of an instruction number, an architecture register number and an old physical register number.

2.   A processor having a register renaming function as set forth in claim 1, wherein said register body comprises a logical register capable of being referred on a program, and said caching register comprises an inner register configured to hold a part of said logical register, said register transfer instruction issuing part comprising a converting part for converting it into an inner register number, which is used by said logical register and said inner register, and a code producing part configured to produce a code in the same form as that of a processor inner instruction code for transferring data between said logical register and said inner register.

3.   A processor having a register renaming function as set forth in claim 1, which further comprises a pre-decoding part configured to pre-decode an instruction from said instruction fetch part to an instruction code.

4.   A processor having a register renaming function as set forth in claim 3, wherein a register instruction inserting unit is configured to insert a load register instruction and a store resister instruction by said pre-decoding part, said instruction insertion determining part and said register transfer instruction issuing part, to issue an instruction.

5.   A processor having a register renaming function as
set forth in claim 4, wherein said register instruction
insertion unit comprises: an inner instruction holding part
configured to hold said inner instruction information; a
pre-decoding part configured to fetch register number
information from an instruction code supplied from said
instruction fetch part; an insertion instruction register
number producing part as said instruction insertion
determining part configured to compare said register number
information, which is supplied from said pre-decoding part,
with a logical register number, which is stored in a TAG
region of the inner instruction information held by said
inner instruction holding part, to produce a register number
of an insertion instruction; and a load/store register
instruction issuing part as said register transfer
instruction issuing part configured to issue a load/store
register instruction on the basis of the register number
of said insertion instruction produced by the insertion
instruction register number producing part.

6.   A processor having a register renaming function as
set forth in claim 5, which further comprises an instruction
insertion control part configured to add an instruction
from said load/store register instruction issuing part
before the instruction supplied from said instruction fetch
part, to the added instruction to said instruction decoding
part on the basis of said load/store register instruction
issuing part, said instruction insertion control part being
provided between said instruction fetch part and said
instruction decoding part.

7.   A processor having a register renaming function,
comprising:
        an instruction fetch part configured to fetch an
instruction;
        a decoding part configured to decode an instruction

code from the instruction fetched by the instruction fetch part;

a register part configured to hold data corresponding to a register number indicated by the instruction code decoded by the decoding part;

a register body configured to hold data corresponding to a register number indicated by said instruction code, and including a logical register capable of being referred on a program;

a caching register configured to cache the contents held by said register body, and including an inner register configured to hold a part of said logical register;

an inner instruction information holding part configured to hold information on a state of an inner instruction including a logical register number and a caching register number, which are held by said caching register by an instruction from said instruction fetch part;

an instruction insertion determining part configured to compare an instruction code, which is obtained by pre-decoding the instruction from said instruction fetch part, with information on a state of the inner instruction, which is held by said inner instruction information holding part, to determine whether the inner instruction is to be inserted; and

a register transfer instruction issuing part configured to issue a register transfer instruction for transferring inner data between said caching register and said register body when said instruction insertion determining part determines that the inner transfer instruction is to be inserted, and comprising a converting part configured to convert it into an inner register number, which is used by said logical register and said inner register, and a code producing part configured to produce a code in the same form as that of a processor inner instruction code for transferring data between said logical register and said inner register,

thereby the processor having a register renaming function for sequentially rewriting the contents of a register alias table using a reorder buffer and a physical register free list, said reorder buffer holding a correspondence of a logical register number to its physical register number, which are included in the decoded instruction code, in a register alias table and storing an assignable number of the physical register number in the physical register free list to store a correspondence of an instruction number, an architecture register number and an old physical register number.

8.   A processor having a register renaming function as set forth in claim 7, which further comprises a pre-decoding part configured to pre-decode an instruction from said instruction fetch part to an instruction code.

9.   A processor having a register renaming function as set forth in claim 8, wherein a register instruction inserting unit is configured to insert a load register instruction and a store resister instruction by said pre-decoding part, said instruction insertion determining part and said register transfer instruction issuing part, to issue an instruction.

10.   A processor having a register renaming function as set forth in claim 9, wherein said register instruction insertion unit comprises: an inner instruction holding part configured to hold said inner instruction information; a pre-decoding part configured to fetch register number information from an instruction code supplied from said instruction fetch part; an insertion instruction register number producing part as said instruction insertion determining part configured to compare said register number information, which is supplied from said pre-decoding part, with a logical register number, which is stored in a TAG

region of the inner instruction information held by said inner instruction holding part, to produce a register number of an insertion instruction; and a load/store register instruction issuing part as said register transfer instruction issuing part configured to issue a load/store register instruction on the basis of the register number of said insertion instruction produced by the insertion instruction register number producing part.

11.   A processor having a register renaming function as set forth in claim 10, which further comprises an instruction insertion control part configured to add an instruction from said load/store register instruction issuing part before the instruction supplied from said instruction fetch part, to the added instruction to said instruction decoding part on the basis of said load/store register instruction issuing part, said instruction insertion control part being provided between said instruction fetch part and said instruction decoding part.

12.   A processor having a register renaming function, comprising:

an instruction fetch part configured to fetch an instruction;

a decoding part configured to decode an instruction code from the instruction fetched by the instruction fetch part;

a register part configured to hold data corresponding to a register number indicated by the instruction code decoded by the decoding part;

a register body configured to hold data corresponding to a register number indicated by said instruction code;

a caching register configured to cache the contents held by said register body;

an inner instruction information holding part

configured to hold information on a state of an inner instruction including a logical register number and a caching register number, which are held by said caching register by an instruction from said instruction fetch part;

an instruction insertion determining part configured to compare an instruction code, which is obtained by pre-decoding the instruction from said instruction fetch part, with information on a state of the inner instruction, which is held by said inner instruction information holding part, to determine whether the inner instruction is to be inserted;

a register transfer instruction issuing part configured to issue a register transfer instruction for transferring inner data between said caching register and said register body when said instruction insertion determining part determines that the inner transfer instruction is to be inserted; and

a pre-decoding part configured to pre-decode an instruction from said instruction fetch part to an instruction code,

thereby the processor having a register renaming function for sequentially rewriting the contents of a register alias table using a reorder buffer and a physical register free list, said reorder buffer holding a correspondence of a logical register number to its physical register number, which are included in the decoded instruction code, in a register alias table and storing an assignable number of the physical register number in the physical register free list to store a correspondence of an instruction number, an architecture register number and an old physical register number.

13.   A processor having a register renaming function as set forth in claim 12, wherein said register body comprises a logical register capable of being referred on a program, and said caching register comprises an inner register for

holding a part of said logical register, said register transfer instruction issuing part comprising a converting part for converting it into an inner register number, which is used by said logical register and said inner register, and a code producing part for producing a code in the same form as that of a processor inner instruction code for transferring data between said logical register and said inner register.

14.   A processor having a register renaming function as set forth in claim 13, wherein a register instruction inserting unit is configured to insert a load register instruction and a store resister instruction by said pre-decoding part, said instruction insertion determining part and said register transfer instruction issuing part, to issue an instruction.

15.   A processor having a register renaming function as set forth in claim 14, wherein said register instruction insertion unit comprises: an inner instruction holding part configured to hold said inner instruction information; a pre-decoding part configured to fetch register number information from an instruction code supplied from said instruction fetch part; an insertion instruction register number producing part as said instruction insertion determining part configured to compare said register number information, which is supplied from said pre-decoding part, with a logical register number, which is stored in a TAG region of the inner instruction information held by said inner instruction holding part, to produce a register number of an insertion instruction; and a load/store register instruction issuing part as said register transfer instruction issuing part configured to issue a load/store register instruction on the basis of the register number of said insertion instruction produced by the insertion instruction register number producing part.

16.   A processor having a register renaming function as set forth in claim 15, which further comprises an instruction insertion control part configured to add an instruction from said load/store register instruction issuing part before the instruction supplied from said instruction fetch part, to the added instruction to said instruction decoding part on the basis of said load/store register instruction issuing part, said instruction insertion control part being provided between said instruction fetch part and said instruction decoding part.